IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A non-volatile semiconductor memory device comprising:

(1) a memory cell array which comprises a NAND cell, said NAND cell comprising:

a plurality of memory transistors connected in series, each memory transistor comprising a charge storage layer and a control gate[[;]],

one end of the NAND cell being connected to a bit line through a first select gate transistor, and

the other end of the NAND cell being connected to a common source line through a second select gate transistor;

~~a first select gate transistor through which said series connected plurality of memory transistors is connected at one end to a bit line; and~~

~~a second select gate transistor through which said series connected plurality of memory transistors is connected at the other end to a common source line,~~

~~wherein in a data write mode, a write voltage is applied to a control gate of a selected one of said plurality of memory transistors of said NAND cell, and a reference voltage is applied to respective control gates of the two memory transistors each adjacent to said selected memory transistor, to thereby turn off the one of said two adjacent memory transistors on the common source line side, and to turn off or on the one of the two adjacent memory transistors on the bit line side depending upon whether data 1 or 0 is applied to the bit line;~~ and

(2) a voltage applying circuit for, when a second one of said memory transistors of said NAND cell counted from the bit line side is selected in the data write mode, applying a

write voltage to a control gate of said second memory transistor ~~from the bit line side~~, applying a reference voltage to a control gate of a third memory transistor, which being non-selected, counted from the bit line side, applying a [[first]] medium voltage lower than the write voltage ~~and higher than the reference voltage~~ to a control gate of a first memory transistor, which being non-selected, counted from said ~~common source~~ bit line side, and ~~a second~~ applying the medium voltage ~~lower than the write voltage and higher than the reference voltage~~ to at least one of the remaining memory transistors, which being non-selected.

Claim 2 (Currently Amended): The non-volatile semiconductor memory device according to claim 1, wherein said voltage applying circuit applies the ~~second~~ medium voltage to all the respective remaining memory transistors, which being non-selected, in said NAND cell.

Claim 3 (Currently Amended): The non-volatile semiconductor memory device according to claim 1, wherein said voltage applying circuit are arranged in such a way that, when a second one of said plurality of memory transistors counted from said common source line side is selected in the write mode, a write voltage is applied to the control gate of said second memory transistor, a reference voltage is applied to a control gate of a third memory transistor, which being non-selected, counted from the common source line side, the [[first]] medium voltage is applied to a control gate of a first memory transistor, which being non-selected, counted from the common source line side, and the ~~second~~ medium voltage is applied to at least one of control gates of the remaining memory transistors, which being non-selected.

Claim 4 (Currently Amended): The non-volatile semiconductor memory device ~~According~~ according to claim 3, wherein said voltage applying circuit applies the ~~second~~ medium voltage to the respective control gates of the remaining memory transistors, which being non-selected, of said NAND cell.

Claims 5-7 (Canceled).

Claim 8 (Original): The non-volatile semiconductor memory device according to claim 1, wherein said memory cell array comprises:

a NAND cell block comprising a plurality of said NAND cells arranged in a row direction and each connected to a respective one of a plurality of bit lines;

a first select gate line connected in common to the gates of said first select gate transistors of said plurality of NAND cells; and

a second select gate line connected in common to the gates of said second select gate transistors of said plurality of NAND cells,

wherein in the write mode, a channel of each said NAND cell is precharged depending upon data applied to a corresponding one of the bit lines, to thereby write data into said plurality of memory transistors connected to a selected control gate line.

Claim 9 (Original): The non-volatile semiconductor memory device according to claim 8, wherein:

said memory device has an erasure mode, which being performed prior to the write mode, in said erasure mode, data stored in said plurality of memory transistors of said NAND

cell block is erased collectively to set said plurality of memory transistors to first data state of a low threshold;

said writing operation in the write mode is performed so as to precharge the channels of said respective NAND cells in accordance with first or second write data from said respective corresponding bit lines,

in each said NAND cell precharged with the first data, the channel of the each memory transistor, which being connected to said selected control gate line, is placed in a floating state, so that, when the write voltage is applied, the each channel in the floating state of the each memory transistor is boosted due to the capacitive coupling to the control gate, to thereby inhibit charge injection into the each charge storage layer; and

in each said NAND cell precharged with the second data, the channel of the each memory transistor, which being connected to said selected control gate line, is held at a low potential, to thereby allow charges to be injected into the charge storage layer of the each memory transistor.

Claim 10 (Currently Amended): A non-volatile semiconductor memory device comprising:

(1) a memory cell array which comprises a NAND cell, said NAND cell comprising:

a plurality of memory transistors connected in series, each memory transistor comprising a charge storage layer and a control gate[[;]],

<u>one end of the NAND cell being connected to a bit line through a first select gate transistor, and</u>

<u>the other end of the NAND cell being connected to a common source line through a second select gate transistor;</u>

~~a first select gate transistor through which said series connected plurality of memory transistors is connected at one end to a bit line; and~~

~~a second select gate transistor through which said series connected plurality of memory transistors is connected at the other end to a common source line,~~

~~wherein in a data write mode, a write voltage is applied to a control gate of a selected one of said plurality of memory transistors, of said NAND cell, and a reference voltage is applied to respective control gates of the two memory transistors each adjacent to said selected memory transistor, to thereby turn off the one of said two adjacent memory transistors on the common source line side, and to turn off or on the one of the two adjacent memory transistors on the bit line side depending upon whether data 1 or 0 is applied to the bit line;~~ and

(2) a voltage applying circuit for, when a second one of said memory transistors of said NAND cell counted from the common source line side is selected in the data write mode, applying a write voltage to a control gate of said second memory transistor counted from the common source line side, applying a reference voltage to a control gate of a third memory transistor, which being non-selected, counted from the common source line side, applying [[first]] a medium voltage lower than the write voltage ~~and higher than the reference voltage~~ to a control gate of a first memory transistor, which being non-selected, counted from said common source line side, and applying the ~~a second~~ medium voltage ~~lower than the write voltage and higher than the reference voltage~~ to at least one of the remaining memory transistors, which being non-selected.

Claims 11-13 (Canceled).

Claim 14 (Original): The non-volatile semiconductor memory device according to claim 10, wherein said memory cell array comprises:

a NAND cell block comprising a plurality of said NAND cells arranged in a row direction and each connected to a respective one of a plurality of bit lines;

a first select gate line connected in common to the gates of said first select gate transistors of said plurality of NAND cells; and

a second select gate line connected in common to the gates of said second select gate transistors of said plurality of NAND cells,

wherein in the write mode, a channel of each said NAND cell is precharged depending upon data applied to a corresponding one of the bit lines to thereby write data into said plurality of memory transistors connected to a selected control gate line.

Claim 15 (Original): The non-volatile semiconductor memory device according to claim 14, wherein:

said memory device has an erasure mode, which being performed prior to the write mode, in said erasure mode, data stored in said plurality of memory transistors of said NAND cell block is erased collectively to set said plurality of memory transistors to first data state of a low threshold;

said writing operation in the write mode is performed so as to precharge the channels of said respective NAND cells in accordance with first or second write data from said respective corresponding bit lines,

in each said NAND cell precharged with the first data, the channel of the each memory transistor, which being connected to said selected control gate line, is placed in a floating state, so that, when the write voltage is applied, the each channel in the floating state

of the each memory transistor is boosted due to the capacitive coupling to the control gate, to thereby inhibit charge injection into the each charge storage layer; and

in each said NAND cell precharged with the second data, the channel of the each memory transistor, which being connected to said selected control gate line, is held at a low potential, to thereby allow charges to be injected into the charge storage layer of the each memory transistor.

Claim 16 (Currently Amended): A non-volatile semiconductor memory device comprising:

(1) a memory cell array which comprises a NAND cell, said NAND cell comprising:

a plurality of memory transistors connected in series, each memory transistor comprising a charge storage layer and a control gate[[;]],

one end of the NAND cell being connected to a bit line through a first select gate transistor, and

the other end of the NAND cell being connected to a common source line through a second select gate transistor;

~~a first select gate transistor through which said series connected plurality of memory transistors is connected at one end to a bit line; and~~

~~a second select gate transistor through which said series connected plurality of memory transistors is connected at the other end to a common line;~~ and

(2) a voltage applying circuit for, when a K-th one of said plurality of memory transistors of said NAND cell counted from the bit line side is selected in a write mode,

applying a write voltage to a control gate of said K-th memory transistor,

applying a reference voltage to control gates of two (K-m)th and ~~(K+m)th~~ (K+n)th memory transistors (where m and n are integers at least one of which is 2 or more), which being non-selected, counted from the bit line side, to thereby turn off said (K+n)th memory transistor and to turn off or on said (K-m)th memory transistor depending upon data "1" or ~~"0" applied~~ "0" applied to the bit line[[;]],

said selected memory transistor and at least any one of two memory transistors disposed one adjacent to each side of said selected memory transistor intervening between said two (K-m)th and (K+n)th memory transistors, which being non-selected[[;]],

applying a first medium voltage lower than the write voltage and higher than the reference voltage to the control gates of the memory transistors, which being non-selected, intervening between said two memory transistors, which being non-selected[[;]], and

applying a second medium voltage lower than the write voltage and higher than the reference voltage to the control gate of at least one of the memory transistors, which being non-selected, on the bit line side from the (K-m)th memory transistor and to the control gate of at least one of the memory transistors, which being non-selected, on the common source line side from the (K+n)th memory transistor.

Claim 17 (Currently Amended): The non-volatile semiconductor memory device according to claim 16, wherein K is 2, and the first or second medium voltage is applied to the respective control [[gates]] gate of said memory ~~transistors~~ transistor on said bit line side from said selected memory transistor.

Claim 18 (Currently Amended): The non-volatile semiconductor memory device according to claim 16, wherein when said selected memory transistor is a second one counted from the common source line side, the first or second medium voltage is applied to the respective control [[gates]] gate of said memory ~~transistors~~ transistor, which being non-selected, on the common source line side from said selected memory transistor.

Claim 19 (Currently Amended): The non-volatile semiconductor memory device according to claim 16, wherein the second medium voltage is applied to the respective control gates of said memory transistors on the bit line side from said (K-m)th memory transistor and to [[to]] the respective control gates of said memory transistors on the common source line side from said (K+n)th memory transistor.

Claim 20 (Original): The non-volatile semiconductor memory device according to claim 16, wherein the first medium voltage is set to a voltage equal to the second medium voltage.

Claim 21 (Original): The non-volatile semiconductor memory device according to claim 16, wherein the first medium voltage is set to a voltage higher than the second medium voltage.

Claim 22 (Original): The non-volatile semiconductor memory device according to claim 16, wherein the first medium voltage is set to a voltage lower than the second medium voltage.

Claim 23 (Original): The non-volatile semiconductor memory device according to claim 16, wherein said memory cell array comprises:

a NAND cell block comprising a plurality of said NAND cells arranged in a row direction and each connected to a respective one of a plurality of bit lines;

a first select gate line connected in common to the gates of said first select gate transistors of said plurality of NAND cells; and

a second select gate line connected in common to the gates of said second select gate transistors of said plurality of NAND cells,

wherein in the write mode, a channel of each said NAND cell is precharged depending upon data applied to a corresponding one of the bit lines to thereby write data into said plurality of memory transistors connected to a selected control gate line.

Claim 24 (New): A non-volatile semiconductor memory device comprising:

(1) a memory cell array which comprises a NAND cell, said NAND cell comprising:

a plurality of memory transistors connected in series, each memory transistor comprising a charge storage layer and a control gate,

one end of the NAND cell being connected to a bit line through a first select gate transistor, and

the other end of the NAND cell being connected to a common source line through a second select gate transistor; and

(2) a voltage applying circuit for, when a second one of said memory transistors of said NAND cell counted from the bit line side is selected in the data write mode, applying a write voltage to a control gate of said second memory transistor, applying a reference voltage to a control gate of a third memory transistor, which is non-selected, counted from the bit line

side, applying a first medium voltage lower than the write voltage and higher than the reference voltage to a control gate of a first memory transistor, which is non-selected, counted from said bit line side, and applying a second medium voltage lower than the write voltage and higher than the reference voltage to at least one of the remaining memory transistors, which is non-selected.

Claim 25 (New): The non-volatile semiconductor memory device according to claim 24, wherein said voltage applying circuit applies the second medium voltage to all the respective remaining memory transistors, which are non-selected, in said NAND cell.

Claim 26 (New): The non-volatile semiconductor memory device according to claim 24, wherein said voltage applying circuit are arranged in such a way that, when a second one of said plurality of memory transistors from said common source line side is selected in the write mode, a write voltage is applied to the control gate of said second memory transistor, a reference voltage is applied to a control gate of a third memory transistor, which is non-selected, counted from the common source line side, the first medium voltage is applied to a control gate of a first memory transistor, which is non-selected, counted from the common source line side, and the second medium voltage is applied to at least one of control gates of the remaining memory transistors, which are non-selected.

Claim 27 (New): The non-volatile semiconductor memory device according to claim 26, wherein said voltage applying circuit applies the second medium voltage to the respective control gates of the remaining memory transistors, which are non-selected, of said NAND cell.

Claim 28 (New): The non-volatile semiconductor memory device according to claim 24, wherein the first medium voltage is set equal to the second medium voltage.

Claim 29 (New): The non-volatile semiconductor memory device according to claim 24, wherein the first medium voltage is set higher than the second medium voltage..

Claim 30 (New): The non-volatile semiconductor memory device according to claim 24, wherein the first medium voltage is set lower than the second medium voltage.

Claim 31 (New): The non-volatile semiconductor memory device according to claim 24, wherein said memory cell array comprises:

a NAND cell block comprising a plurality of said NAND cells arranged in a row direction and each connected to a respective one of a plurality of bit lines;

a first select gate line connected in common to the gates of said first select gate transistors of said plurality of NAND cells; and

a second select gate line connected in common to the gates of said second select gate transistors of said plurality of NAND cells,

wherein in the write mode, a channel of each said NAND cell is precharged depending upon data applied to a corresponding one of the bit lines, to thereby write data into said plurality of memory transistors connected to a selected control gate line.

Claim 32 (New): The non-volatile semiconductor memory device according to claim 31, wherein:

said memory device has an erasure mode, which being performed prior to the write mode, in said erasure mode, data stored in said plurality of memory transistors of said NAND cell block is erased collectively to set said plurality of memory transistors to first data state of a low threshold;

said writing operation in the write mode is performed so as to precharge the channels of said respective NAND cells in accordance with first or second write data from said respective corresponding bit lines;

in each said NAND cell precharged with the first data, the channel of each memory transistor, which being connected to said selected control gate line, is placed in a floating state, so that, when the write voltage is applied, each channel in the floating state of each said memory transistor is boosted due to the capacitive coupling to the control gate, to thereby inhibit charge injection into each said charge storage layer; and

in each said NAND cell precharged with the second data, the channel of each said memory transistor, which being connected to said selected control gate line, is held at a low potential, to thereby allow charges to be injected into the charge storage layer of each said memory transistor.